



深圳市矽源特科技有限公司

ShenZhen ChipSourceTek Technology Co. ,Ltd.

CST8002D LOW-EMI Class AB Audio Power Amplifier

矽源特科技
ChipSourceTek

CST8002D
User Manual

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V1.2



CST8002D

3W LOW-EMI Class AB Audio Power Amplifier

CST8002D General Description:

The CST8002D is an audio power amplifier primarily designed for demanding applications in low-power portable systems. It is capable of delivering 3 watts of continuous average power to an 3 BTL load with less than 10% distortion (THD) from a 5VDC power supply. the CST8002D does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for audio systems and other low voltage applications where minimal power consumption is a primary requirement. The CST8002D features a low-power consumption shutdown mode. the CST8002D contains advanced pop & click circuitry which eliminates noise which would otherwise occur during turn-on and turn-off transitions. The CST8002D is unity-gain stable and can be configured by external gain-setting resistors. The CST8002D can provide your USB subwoofer, radio, MP3 player, and loudspeaker perfect solution.

CST8002D Features:

VDD=5V RL=3 Po=3W THD+N 10%

Wide operating voltage range: 1.5V~5.5V

Improved pop & click circuitry eliminates noise during turn-on and turn-off transitions

Available in space-saving packages: SOP-8

CST8002D Applications:

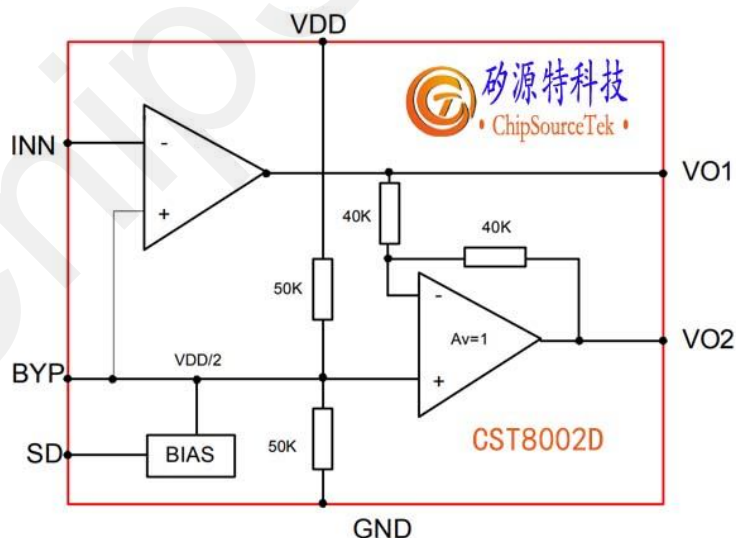
Card inserting speaker, Bluetooth speaker

Handheld game machine

Low voltage audio systems

IPC

CST8002D Block diagram:





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CST8002D Ordering Information:

Part Number	Package Type	Shipping Package	PCS	Note
CST8002D	SOP8	100 Units/real		
CST8002D	SOP8	4000 Units/Tape & Reel		

CST8002D Typical Application Circuit:

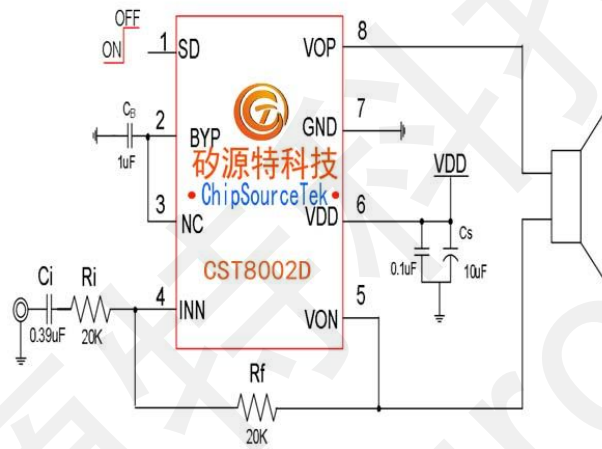


Fig1. The CST8002D Typical Application Circuit

CST8002D Pin Distribution:





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Fig2. Pin Distribution

CST8002D Pin description:

Pin Number	Symbol	Description
1	SD	The device enters in shutdown mode when a high level is applied on this pin
2	BYP	Internal common-mode voltage
3	NC	No Connect
4	INP	Negative input of the first amplifier, receives the audio input signal
5	VON	The negative phase output
6	VDD	Power
7	GND	Ground
8	VOP	The positive phase output

CST8002D Absolute Maximum Ratings:

Absolute Maximum Ratings

Note: In any t htsi n nts beyond the limit value, the performance is not guaranteed.



CST8002D Recommended operating conditions:

Recommended operating conditions

Name	Test Conditions		Min	Max	Units
VDD	Supply Voltage		1.5	5.5	V
VIH	High-level input voltage	SD	1.5		V
VIL	Low-level input voltage	SD		1.2	V

CST8002D Electrical Characteristics :

Symbol	Parameter	Test Conditions		Min	Typical	Max	Units
VDD	Input voltage range			1.8	5	5.5	V
Rdson	Drain-source on-state resistance	VDD=5V			200		m
I(Q)	Quiescent Power Supply Current	VDD= 5V, no load			10		mA
I(SD)	Shutdown Current	VDD=2V to 5.5V			0.5		μA
VOS	Output Offset Voltage	VIN = 0V			10	50	mV
Po	Output Power	THD+N=10%,f=1kHz, RL=3	VDD=5V		3		W
		THD+N=1%,f=1kHz, RL=3			2.4		
THD+N	Total Harmonic Distortion+Noise	VDD=5V,PO=1W, RL=4, f=1kHz			0.1		%

CST8002D APPLICATION INFORMATION:

The input resistance (Ri) selection

The CST8002D contains two stage gains, the first stage gain can be configured by an external input resistor, and the second stage gain is the internal fixation. By choosing the input resistance value can set the gain of the amplifier:

$$A_{VD}=2X(Rf/Ri) \quad (1)$$

Any mismatch between the resistors results in a differential gain error that leads to an increase in THD+N,



decrease in PSRR and CMRR, as well as an increase in output offset voltage. Resistors with a tolerance of 1% or better are recommended. The gain setting resistors should be placed as close to the device as possible. Keeping the input traces close can increase noise rejection in noisy environments. Noise coupled onto the input traces which are physically close to each other will be common mode and easily rejected. Low gain and high voltage signal can make the chip performance more prominent.

The input capacitor C_i selection

In the typical application, an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_i) form a high-pass filter with the corner frequency determined in Equation 5.

$$= \frac{1}{\pi} \quad (2)$$

The value of C_i is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_i is 20k and the specification calls for a flat bass response down to 20Hz. Equation 5 is reconfigured as Equation 6.

$$= \frac{1}{\pi} \quad (3)$$

In this example, C_i is 56.8nF, so one would likely choose a value in the range of 56nF to 1μF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

CST8002D The bypass capacitor (CBYP) selection:

In CST8002D, a capacitor CB (connected to the VBYP pin) is very crucial; it can affect the PSRR and switching noise performance. Generally, the capacitance of the ceramic capacitor CB is 0.033μF ~ 1μF. In addition to minimize the input and output capacitor size, the bypass capacitor size should also be considered in detail. The bypass capacitor CB is used to minimize the system noise.

The selection of the capacitor value on the VBYP terminal is critical for achieving the best device performance. During power up or recovery from the shutdown state, the VBYP capacitor determines the rate at which the amplifier starts up. When the voltage on the VBYP capacitor equals V_{BYP} , the device starts a 40-ms timer. When this timer completes, the outputs start switching. The charge rate of the capacitor is calculated using the standard charging formula for a capacitor, $I=C \times dV/dT$. For example, a 1-μF capacitor on VBYP would take 50ms to reach the value of V_{BYP} and begin a 40ms count before the outputs turn on. This equates to a turn-on time of 90ms for a 1-μF capacitor on the VBYP terminal.

CST8002D BTL Amplifier efficiency :



Power consumption is one of the key indicators for the amplifier, differential output amplifier maximum self power is as follows:

$$= \pi \quad (4)$$

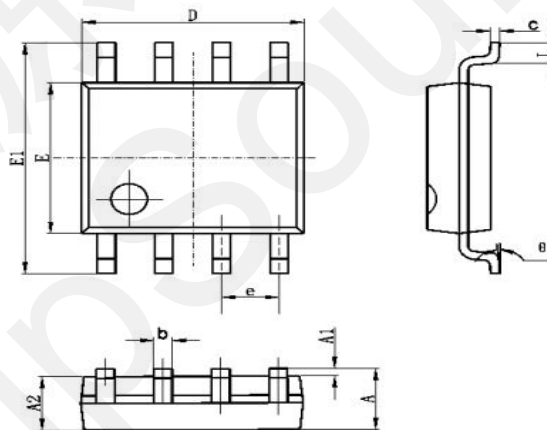
It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding copper foil, the thermal resistance of the application can be reduced from the free air value of θ_{JA} , resulting in higher P_{DMAX} values without thermal shutdown protection circuitry being activated. Additional copper foil can be added to any of the leads connected to the CST8002D. It is especially effective when connected to VDD, GND, and the output pins. Refer to the application information on the CST8002D reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150°C , then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power.

CST8002D Shutdown function:

In order to reduce power consumption while not in use, the CST8002D contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. The SD pin controls the amplifier's shutdown mode, and the amplifier can be shutdown with a high level logic signal to the SD pin.

CST8002D Package Information:

SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



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